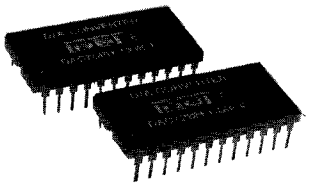
BURR-BROWN®



DAC70BH
DAC72BH

Monolithic 16-Bit DIGITAL-TO-ANALOG CONVERTERS

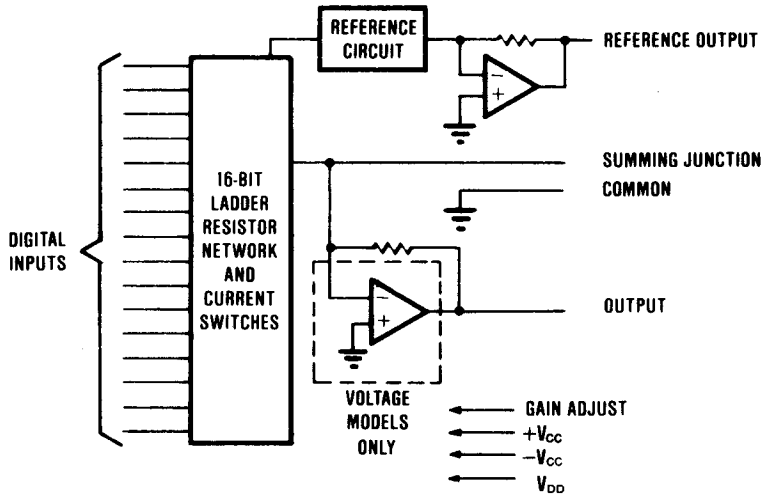
FEATURES

- 16-BIT RESOLUTION
- ±0.003% MAXIMUM NONLINEARITY
- LOW DRIFT ±7ppm/°C, (TYPICAL)
- MONOLITHIC CONSTRUCTION
- EXACT DAC70/72 HYBRID REPLACEMENT
- MONOTONIC (AT 14 BITS) OVER FULL SPECIFICATION TEMPERATURE RANGE
- CURRENT AND VOLTAGE MODELS

DESCRIPTION

The DAC70BH/72BH are complete 16-bit digital-to- analog converters that include a precision buried-zener voltage reference and a low-noise, fast-setting output operational amplifier (voltage output models), all on one small monolithic chip. A combination of current-switch design techniques accomplishes not only 14-bit monotonicity over the entire specified temperature range but also a maximum end-point linearity error of ±0.003% of full-scale range. Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, 54/74HC-compatible over the entire temperature range. Outputs of 0 to +10V, ±10V, 0 to −2mA, and ±1mA are available.

These D/A converters are packaged in hermetic 24-pin ceramic side-brazed packages.



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SBAS160

SPECIFICATIONS

ELECTRICAL

Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC70BH			DAC72BH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT							
DIGITAL INPUT							
Resolution, CSB, COB			16			*	Bits
Digital Inputs[1]: V_{IH}	+2.4		+5.5	*		*	V
V_{IL}	0		+0.4	*		*	V
I_{IH} V_I = +2.7V			+40			*	µA
I_{IL} V_I = +0.4V			−1.6			*	mA
TRANSFER CHARACTERISTICS							
ACCURACY[2]							
Linearity Error At +25°C			±0.003			*	% of FSR[3]
Gain Error[4]: Voltage					±0.05	±0.15	%
Current			±0.05		±0.05	±0.25	%
Offset Error[4]: Voltage, Unipolar					±0.10	±2	mV
Bipolar						±10	mV
Current, Unipolar			±1			*	µA
Bipolar			±1			±5	µA
Monotonicity Temperature Range (14 bits)	−25		+85	*		*	°C
DRIFT (OVER SPECIFIED TEMPERATURE RANGE)							
Total Bipolar Drift (Includes Gain, Offset, and Linearity Drift):[5] Voltage					±5	±11	ppm-of FSR/°C
Current		±10			*	±40	ppm of FSR/°C
Total Error Over Temperature Range:							
Voltage, Unipolar						±0.072	% of FSR
Bipolar						±0.072	% of FSR
Current, Unipolar		±0.12				±0.24	% of FSR
Bipolar		±0.12				±0.24	% of FSR
Gain: Voltage					±5	±20	ppm/°C
Current			±7			±47	ppm/°C
Offset: Voltage, Unipolar					±1	±2	ppm of FSR/°C
Bipolar						±8	ppm of FSR/°C
Current, Unipolar		±1				±1	ppm of FSR/°C
Bipolar			±5			±35	ppm of FSR/°C
Differential Linearity over Temperature		±1				±1	ppm of FSR/°C
Linearity over Temperature			±2			±1	ppm of FSR/°C
SETTLING TIME[6]							
Voltage Models (to ±0.003% of FSR)							
Output: 20V Step					5	10	µs
1LSB Step[7]					3	5	µs
Slew Rate					10		V/µA
Switching Transient[8]					500		mV
Current Models (to ±0.003% of FSR)							
Output, 2mA step: 10Ω to 100Ω load		15				1	µs
1kΩ load		50				3	µs
OUTPUT							
ANALOG OUTPUT							
Voltage Models							
Ranges: CSB					0 to +10		V
COB					±10		V
Output Current				±5			mA
Output Impedance (DC)					0.05		Ω
Short Circuit Duration					Indefinite to Common		
Current Models							
Ranges: CSB		0 to −2			*		mA
COB		±1			*		mA
Output Impedance: Unipolar		4.0			*		kΩ
Bipolar		2.45			*		kΩ
Compliance		±2.5			*		V
INTERNAL VOLTAGE REFERENCE	6.0	6.3	6.6	*	*	*	V
Maximum External Current		±200				±200	µA
Temperature Coefficient of Drift		±7			±10		ppm/°C

ELECTRICAL (CONT)

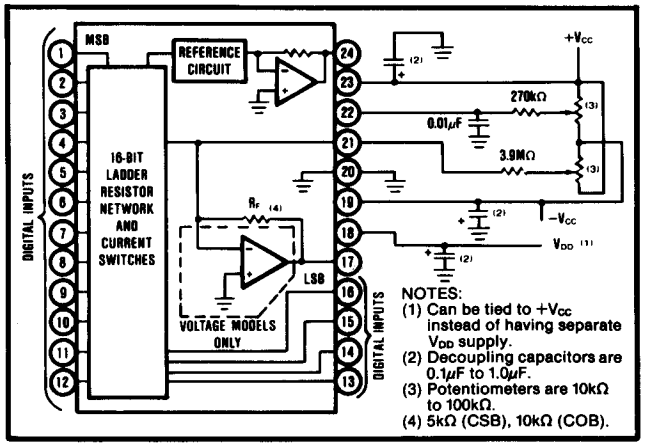
Typical at T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	DAC70BH			DAC72BH			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY SENSITIVITY							
Unipolar Offset: ±15VDC		±.0001			*		% of FSR/% V_{CC}
+5VDC		±.0001			*		% of FSR/% V_{DD}
Bipolar Offset: ±15VDC		±.0004			*		% of FSR/% V_{CC}
+5VDC		±.0001			*		% of FSR/% V_{DD}
Gain: ±15VDC		±0.001			*		% of FSR/% V_{CC}
+5VDC		±.0005			*		% of FSR/% V_{DD}
POWER SUPPLY REQUIREMENTS							
Voltage	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	*	*	*	VDC
Supply Drain: ±15VDC (no load)		±20			*	±30	mA
+5VDC (logic supply)		+5			*	±10	mA
TEMPERATURE RANGE							
Specification	−25		+85	*		*	°C
Storage	−60		+150	*		*	°C

*Specification same as DAC70.

NOTES: (1) Digital inputs are TTL, LSTTL, 54/74C, 54/74HC, and 54/74HTC compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. (2) Current-output models are specified and tested with an external output operational amplifier connected using the internal feedback resistor in all parameters except settling time. (3) FSR means full-scale range and is 20V for the ±10V range (COB-V), 10V for the 0 to +10V range (CSB-V). FSR is 2mA for the ±1mA range (COB-I) and the 0 to −2mA range (CSB-I). (4) Adjustable to zero with external trim potentiometer. (5) With gain and zero errors adjusted to zero at +25°C. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) LSB is for 14-bit resolution. (8) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$.

CONNECTION DIAGRAM

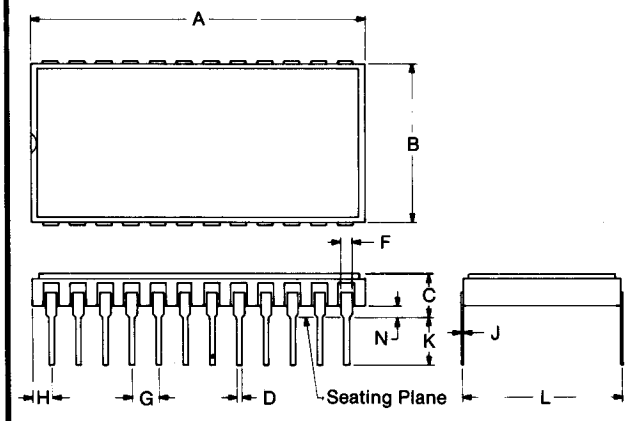


PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
Bit 12	12	Bit 12
Bit 13	13	Bit 13
Bit 14	14	Bit 14
Bit 15	15	Bit 15
(LSB) Bit 16	16	Bit 16 (LSB)
R_F	17	V_{OUT}
+5VDC	18	+5VDC
-15VDC	19	-15VDC
COMMON	20	COMMON
I_{OUT}	21	SUMMING JUNCTION
GAIN ADJUST	22	GAIN ADJUST
+15VDC	23	+15VDC
6.3V REF. OUT	24	6.3V REF. OUT

MECHANICAL

H Package–24-Pin Hermetic Ceramic



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.238	1.262	31.45	32.05
B	.586	.602	14.88	15.29
C	.160	.196	4.06	4.98
D	.016	.020	0.41	0.51
F	.038	.042	0.97	1.07
G	.100 BASIC		2.54 BASIC	
H	.067	.085	1.70	2.16
J	.008	.012	0.20	0.30
K	.170 BASIC		4.32 BASIC	
L	.600 BASIC		15.24 BASIC	
N	.040	.060	1.02	1.52

ABSOLUTE MAXIMUM SPECIFICATIONS

$+V_{CC}$ to Common	0V to +16.5V
$-V_{CC}$ to Common	0V to −16.5V
$+V_{DD}$ to Common	0V to +16.5V
Logic Inputs to Common	0V to V_{DD}
Maximum Power Dissipation	1000mW
Lead Temperature (10s)	300°C

ORDERING INFORMATION

MODELS	
Complementary Offset Binary Coding	
DAC70BH-COB-I	I_{OUT} DAC
DAC70BH-COB-IBI	Burn-in Option[1]
DAC72BH-COB-I	I_{OUT} DAC
DAC72BH-COB-IBI	Burn-in Option[1]
DAC72BH-COB-V	V_{OUT} DAC
DAC72BH-COB-VBI	Burn-in Option[1]
Complementary Straight Binary Coding	
DAC70BH-CSB-I	I_{OUT} DAC
DAC70BH-CSB-IBI	Burn-in Option[1]
DAC72BH-CSB-I	I_{OUT} DAC
DAC72BH-CSB-IBI	Burn-in Option[1]
DAC72BH-CSB-V	V_{OUT} DAC
DAC72BH-CSB-VBI	Burn-in Option[1]

NOTE: 1) 160 hours at 85°C or equivalent. See text.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC70BH/72BH accept complementary digital input codes in either binary format (CSB, Unipolar or COB, Bipolar). The COB models may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output		
	Complementary Straight Binary (CSB)	Complementary Offset Binary (COB)	Complementary Two's Complement (CTC)*
0000_H	+Full Scale	+Full Scale	-1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	-Full Scale
8000_H	+1/2 Full Scale -1LSB	-1LSB	+Full Scale
$FFFF_H$	Zero	-Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity

This specification describes one of the most important measures of performance of a D/A converter. Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity Error

Differential Linearity Error (DLE) of a D/A converter is the deviation from an ideal 1LSB change in the output from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output step sizes can be between 1/2LSB and 3/2LSB when the input changes from one adjacent input state to the next. A negative DLE specification of no more than −1LSB (−0.006% for 14-bit resolution) insures monotonicity.

Monotonicity

Monotonicity assures that the analog output will increase or remain the same for increasing input digital codes. The DAC70BH/72BH are specified to be monotonic to 14 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts per million per degree centigrade (ppm/°C). Gain drift is established by : (1) testing the end point differences for each D/A at t_{min}, +25°C and t_{max}; (2) calculating the gain error with respect to the +25°C value; and (3) dividing by the temperature change.

Offset Drift

Offset drift is a measure of the change in the output with $FFFF_H$ applied to the digital inputs over the specified temperature range. The maximum change in offset at t_{min} or t_{max} is referenced to the offset error at +25°C and is divided by the temperature change. This drift is expressed in parts per million of full scale range per degree centigrade (ppm of FSR/°C).

SETTLING TIME

Settling time of the D/A is the total time required for the analog output to settle within an error band around its final value after a change in digital input. Refer to Figure 1 for typical values for this family of products.

Voltage Output

Settling times are specified to ±0.003% of FSR (±1/2LSB for 14 bits) for two input conditions: a full-scale range change of 20V (COB) or 10V (CSB) and a 1LSB change at the "major carry," the point at which the worst-case settling time occurs. (This is the worst-case point since all of the input bits change when going from one code to the next).

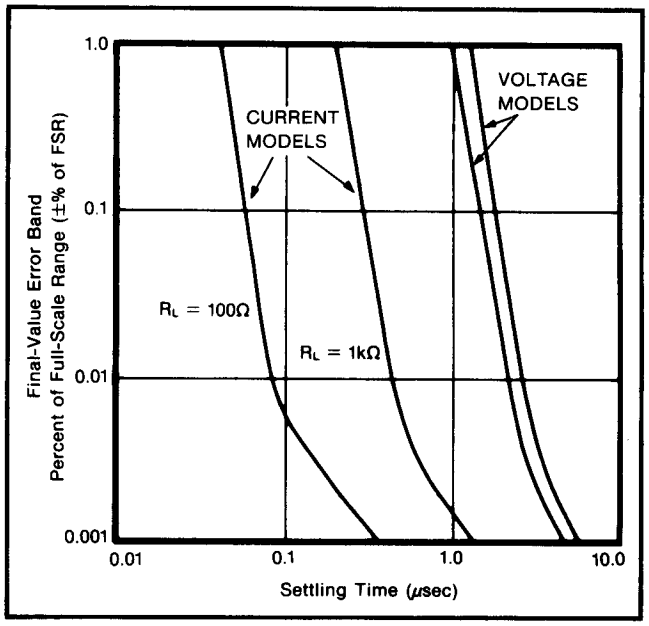


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

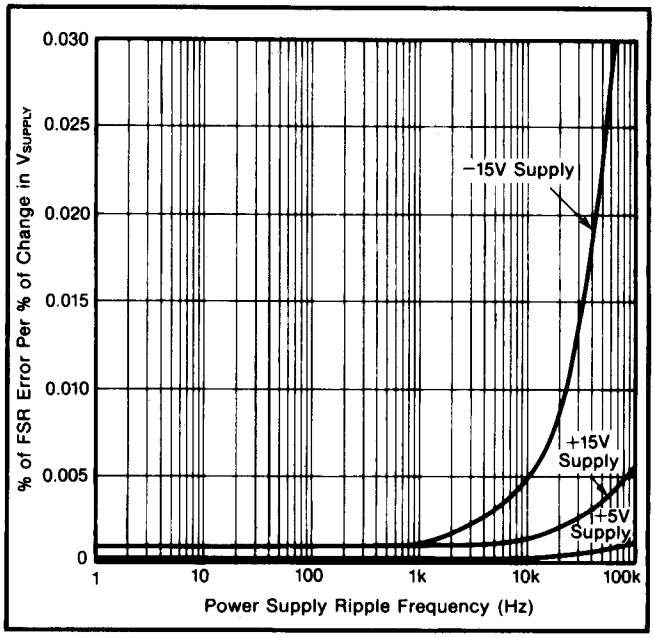


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

Current Output

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω. It is specified this way because the output RC time constant becomes the dominant factor in determining settling time for large resistive loads.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output current pin while still being able to maintain specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a change in a power supply voltage on the D/A converter output. It is defined as a percent of FSR change in the output per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2). It is specified for DC or low frequency changes. The typical performance curve in Figure 2 shows the effect of high frequency changes in power supply voltages.

REFERENCE SUPPLY

All models have an internal low-noise +6.3V reference voltage derived from an on-chip buried zener diode. This reference voltage is available to the user. A minimum of 200μA is available for external loads. Since the output impedance of the reference output is typically 1Ω, the external load should remain constant.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the Bipolar Offset (connected internally to the reference) from load variations.

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC70BH/72BH family of products. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add " BI" to the base model number.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC70BH/72BH. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external offset and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 510kΩ resistors (20% carbon or better) should be located close to the DAC70BH/72BH to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ. A 0.001μF to 0.01μF ceramic capacitor should be connected from Gain Adjust (pin 22) to common to prevent noise pickup. Refer to

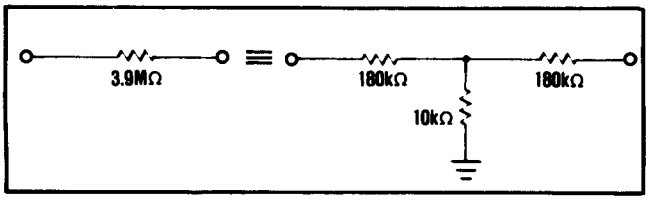


FIGURE 3. Equivalent Resistances.

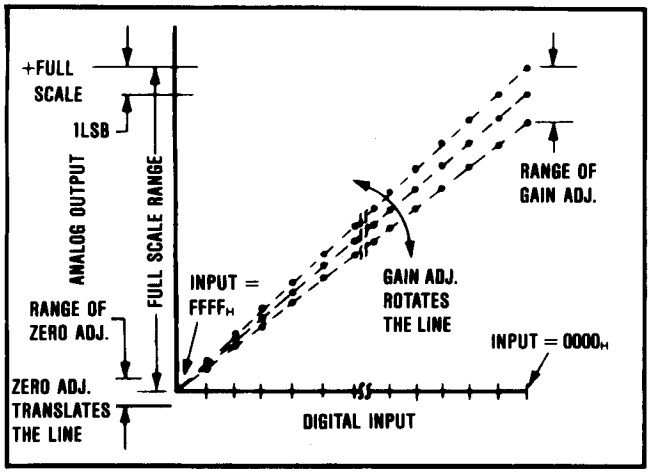


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

Figures 4 and 5 for relationship of offset and gain adjustments to unipolar and bipolar D/A converters.

OFFSET ADJUSTMENT

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the offset potentiometer for zero output.

For bipolar (COB) configurations, apply the digital input code that should produce the maximum negative output voltage. The COB model is internally connected for a 20V FSR range where the maximum negative output voltage is −10V. See Table II for corresponding codes and the Connection Diagram for offset adjustment connections. Offset adjust should be made prior to gain adjust.

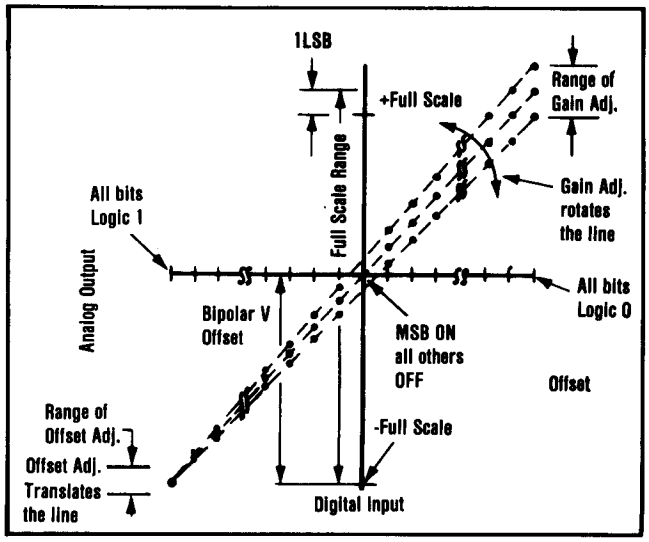


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output voltage. Adjust the gain potentiomenter for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagram for gain adjustment connections.

INSTALLATION CONSIDERATIONS

This D/A converter family is laser-trimmed to 14-bit linearity. The design of the device makes the 16-bit resolution available. If 16-bit resolution is not required, bit 15 and 16 should be connected to V_{DD} through a single 1kΩ resistor.

Due to the extremely-high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and

TABLE II. Digital Input and Analog Output Relationships.

VOLTAGE OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μV)	153	305	610	305	610	1224
0000$_H$ (V)	+9.99985	+9.99969	+9.99939	+9.99969	+9.99939	+9.99878
FFFF$_H$ (V)	0	0	0	−10.0000	−10.0000	−10.0000
CURRENT OUTPUT MODELS						
	Analog Output					
	Unipolar			Bipolar		
Digital Input Code	16-bit	15-bit	14-bit	16-bit	15-bit	14-bit
One LSB (μA)	0.031	0.061	0.122	0.031	0.061	0.122
0000$_H$ (mA)	−1.99997	−1.99994	−1.99988	−0.99997	−0.99994	−0.99988
FFFF$_H$ (mA)	0	0	0	+1.00000	+1.00000	+1.00000

connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Neglecting contact resistance, less than 18 inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 6, 7, and 8, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance R_L is constant, R_2, simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at Common, and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at the output pin. Sensing the output voltage at the system ground point is permissible with the DAC70 family because the D/A converter is designed to have a constant return current of approximately 2mA flowing from Common. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times$ 2mA) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 6, 7, and 8.

Figures 7 and 8 show two methods of connecting the current output models with external precision output op amps. By sensing the output voltage at the load resistor

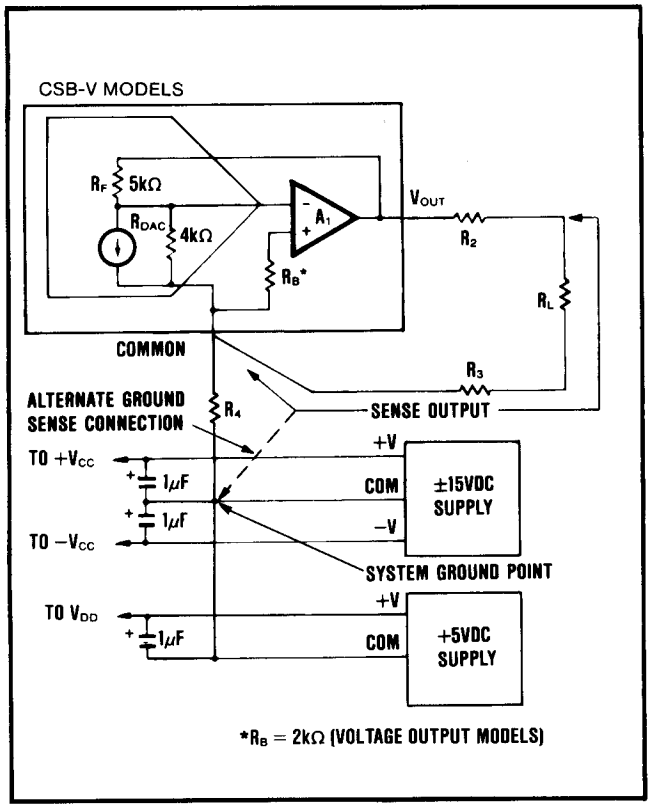


FIGURE 6. Output Circuit for Voltage Models.

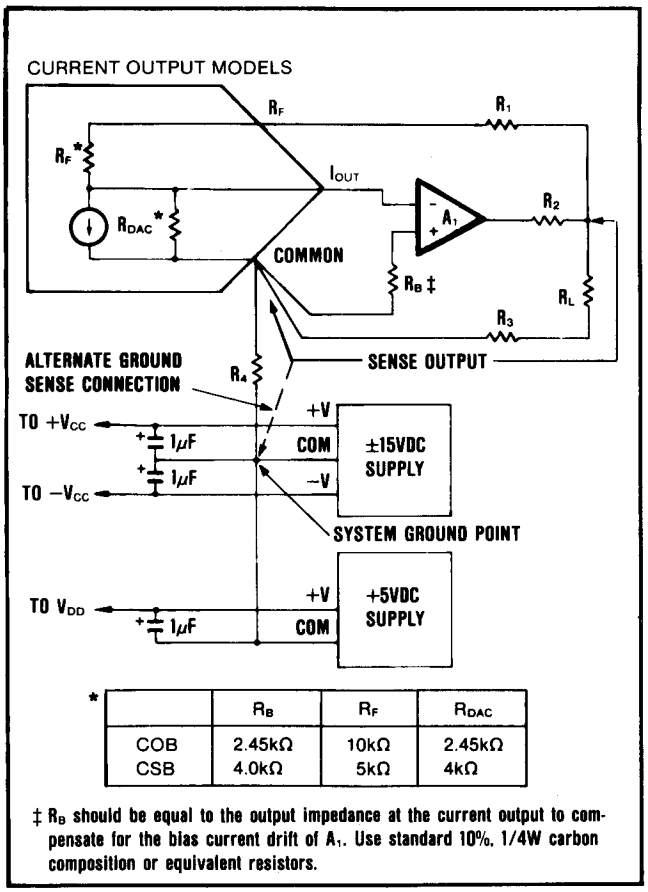


FIGURE 7. Preferred External Op Amp Configuration.

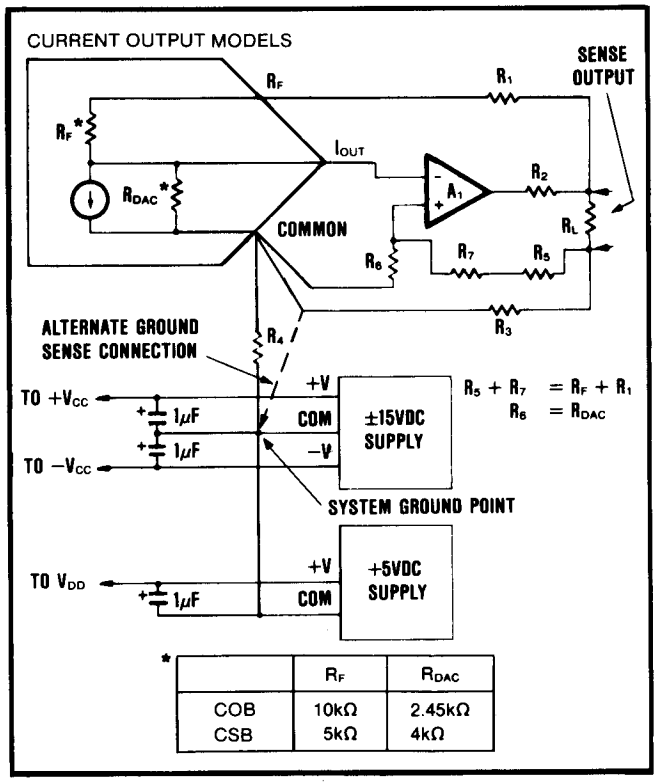


FIGURE 8. Differential Sensing Output Op Amp Configuration.

(i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain.

If the output cannot be sensed at Common or the system ground point as mentioned above, the differential output circuit shown in Figure 8 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 8 can be reduced to the one shown in Figure 7. Again the effect of R_4 is negligible.The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a single lead and its return conductor are wired close together, they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT DACs

The DAC70BH/72BH current output models will drive the summing junction of an op amp to produce an output voltage as shown in Figure 9. Use of the internal feedback resistor is required to obtain specified gain accuracy and low gain drift.

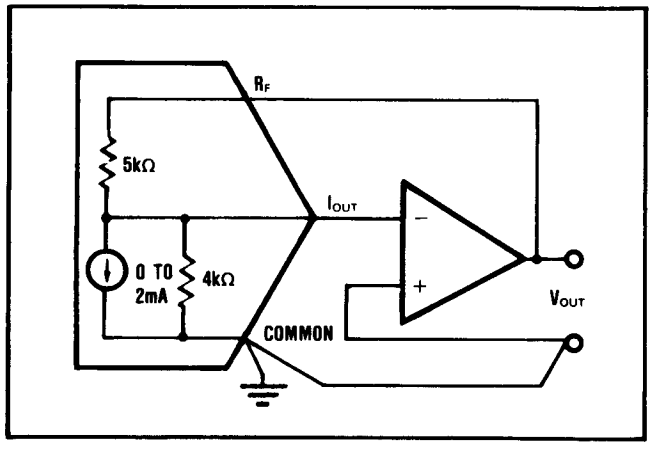


FIGURE 9. External Op Amp Using Internal Feedback Resistors.

Current output models can be scaled for any desired voltage range with an external feedback resistor, but at the expense of increased drifts of up to ±50ppm/°C. The resistors in the D/A converter ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 10.

OUTPUTS LARGER THAN 20-VOLT RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 11). Use protection diodes as shown when a high voltage op amp is used.

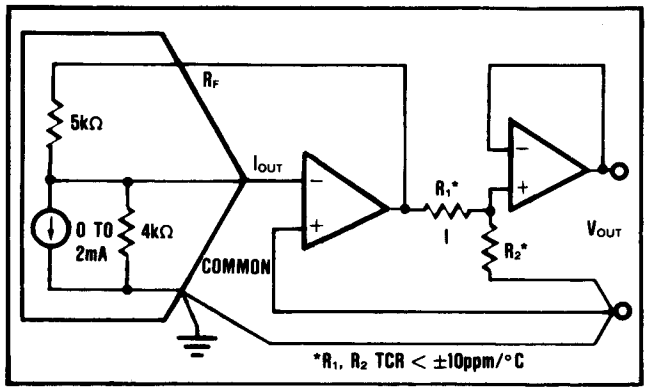


FIGURE 10. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift.

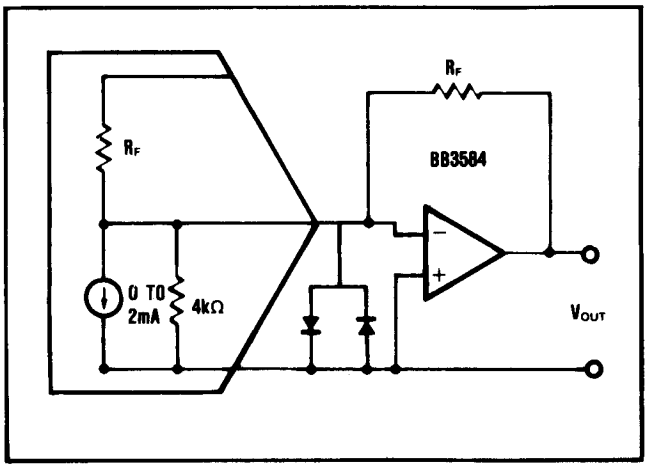


FIGURE 11. External Op Amp Using External Feedback Resistors.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC70BH-CSB-I	OBSOLETE	ZZ (BB)	ZZ176	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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